What is claimed is:

1. A method for on-board programming and/or In-System Configuration of a flash memory on a circuit board, comprising:

controlling inputs of the flash memory with an ASIC mounted on the circuit board via individual memory cells of a Boundary Scan register for activation or deactivation of a write operation, wherein

an architecture description of the ASIC and the flash memory to be programmed and the data format of the program and configuration data are provided in a file,

the printed circuit board is configured to be controlled via an interface for input or output of standard bus signals and for input of the control signals of the ASIC, and

the data of the network list or the circuit diagram which define the configuration of the interface between the flash memory to be programmed and the ASIC is provided in additional files.

2. The method according to claim 1, wherein the ASIC and flash memory to be programmed are controlled as a continuous unit.

3. The method according to claim 2, wherein a programming algorithm for programming the flash memory is created automatically by access to the additional file.

4. The method according to claim 1, further comprising simultaneously programming of a number of flash memories on the circuit board via the interface.

5. The method according to claim 1, further comprising providing a data register for buffering the address and control data occurring during burst mode operation, which is connected to the outputs of the ASIC provided for programming the flash memory.

6. A parallel interface for on-board programming and/or In-System Configuration of a flash memory on a printed circuit board by controlling individual inputs of the flash memory with an ASIC mounted on the printed circuit board via memory cells of a Boundary Scan register for activating or deactivating a write operation, wherein the parallel interface is formed by a series connection of a number of memory cells which are part of the Boundary Scan register.

7. A parallel interface for on-board programming and/or In-System Configuration of a flash memory on a printed circuit board by controlling individual inputs of the flash memory with an ASIC mounted on the printed circuit board via memory cells of a Boundary Scan register for activating or deactivating a write operation, wherein the parallel interface is formed by series connection of a number of memory cells of a data register used for In-System Configuration of the flash memory to be programmed.

8. A memory cell of a Boundary Scan register for on-board programming of a flash memory on a printed circuit board by controlling individual inputs of the flash memory with an ASIC mounted on the printed circuit board or activating or deactivating a write operation, comprising:

an input multiplexer for through connecting one of at least two input signals depending on a control signal present at a control signal input, which optionally switches through

a connection from the ASIC or from a signal input for Boundary Scan test data to the flash memory;

a scan or capture flip-flop to buffer the programming data or the Boundary Scan test data received from the ASIC;

an update flip-flop for controlling individual control signal, data and/ or address inputs of the flash memory to initiate or end a write operation; and

an output multiplexer for through connecting one of at least two input signals, depending on a control signal present at a control signal input, which optionally switches through a connection from ASIC or from a signal input for configuration data to flash memory.

9. A memory cell of a data register for In-System Configuration of a flash memory on a printed circuit board by controlling individual inputs of the flash memory with an ASIC mounted on the printed circuit board for activating or deactivating a write operation, comprising:

a scan or capture flip-flop for buffering the configuration data received by the ASIC; and

an output multiplexer for through connecting one of two input signals, depending on a control signal present at a control signal input, which optionally switches through a connection from the ASIC or from a signal input for Boundary Scan test data or from a signal input from configuration data to the flash memory.

10. The memory cell according to claim 9, wherein instead of the output multiplexer an update flip-flop is used for controlling individual control signal, data and/or address inputs of the flash memory in order to trigger or end a write operation.